IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the paragraph on page 2, lines 11-20 with the following paragraph:

-- For example, in digital circuit 1, if second conductive path 12 is of much greater length than first conductive path 8, then a delay may be caused in the feedback loop. If the output of AND gate 10 is delayed, then the value of A may not have been updated when a new value for B arrives at OR gate 6. In another example, it is assumed that second conductive path 12 is much shorter than first conductive path 8 and AND gate 10 has a shorter delay than AND gate 4. In such a scenario, the output of AND gate 4 may be delayed so much that OR gate 6 operates on a new value of AND gate 10 and an old value of AND gate 4. This is known as a min-delay problem. Because there is a race between values of A and B to be input into OR gate ~~22~~ 6, a race resolution mechanism must be used to correctly analyze and describe the operation of digital circuit 1. –

Please replace the paragraph on page 3, lines 1-9 with the following paragraph:

-- For example, if ATPG were used to generate test patterns for digital circuit 1, errors in testing would occur because there is no race resolution mechanism for OR gate ~~22~~ 6. Not only would ATPG assume that one signal is arriving right after the other signal, it would also assume that the order in which signals arrive at OR gate ~~22~~ 6 is arbitrary. Therefore, a test pattern generated by ATPG for digital circuit 1 would lead to errors in testing. In view of the foregoing, it is desirable to have a method and apparatus for modeling delays within a netlist or other circuit model to allow ATPG to generate a test pattern that is able to perform race resolution on circuits that exhibit asynchronous behavior either individually or collectively with other circuit elements. –

Please replace the paragraph on page 6, lines 20-27 with the following paragraph:

-- Figure 3A is a diagram of a model digital circuit 1' for ATPG in accordance with one embodiment of the present invention. In addition to the elements present in the actual physical digital circuit 1, modeled digital circuit 1' further includes a virtual delay element 24 having an input coupled to a virtual clock vclk1 and a virtual delay element 26 having an input coupled to a virtual clock vclk2. Virtual delay element 24 is also coupled to the output of AND gate ~~10~~ 4 and to the input of OR gate 6 along first conductive path 8. Virtual delay element 26 is coupled to the input of AND gate 10 and the output of OR gate 6 along second conductive path 12. --